CLAIMS

What is claimed is:

1. A static logic to dynamic logic interface, comprising:

a delay having a delay input and a delay output; and,

a latch having a clock input, an enable input, a data input for connection to static logic, and a data output for connection to dynamic logic and wherein said delay input and said clock input connect to an inverse of a dynamic logic evaluate clock and said delay output connects to said enable input.

2. The static logic to dynamic logic interface of claim 1 wherein said delay is comprised of a plurality of inverters.

3. The static logic to dynamic logic interface of claim 1 wherein said latch is a transparent latch.

4. The static logic to dynamic logic interface of claim 1 wherein said delay is comprised of a plurality of inverters and said latch is a transparent latch.

5. A method of interfacing static logic and dynamic logic, comprising:

supplying a static logic signal to a data input of a latch having an output;

supplying said output to dynamic logic;

clocking said latch with an inverse of a dynamic logic evaluate clock; and,

enabling said latch with a delayed version of said inverse of said dynamic logic evaluate clock.

6. The method of claim 5 wherein said latch is a transparent latch.

7. The method of claim 5 wherein said delayed version of said inverse of said dynamic logic evaluate clock is generated by supplying a delay element with said said inverse of said dynamic logic evaluate clock.

8. The method of claim 7 wherein said delay element is comprised of a plurality of inverters.

9. A static logic to dynamic logic interface, comprising:

a clock that is the inverse of a second clock that causes dynamic logic to evaluate;

a delay element that generates a delayed clock; and,

a latch having a clock input that receives said clock, an enable input that receives said delayed clock, a data input that interfaces to static logic, and an output that interfaces to dynamic logic.

10. The interface of claim 9 wherein said latch comprises:

a first pass gate having a first pass gate output, said first pass gate receiving said data input and being controlled by said delayed clock; and,

a second pass gate having a second pass gate output that controls a latching node of said latch, said second pass gate receiving said first pass gate output and being controlled by said clock.

11. The interface of claim 11 wherein said latch inverts said latching node of said latch to produce said output.

12. The interface of claim 11 wherein said delay element comprises a plurality of inverters.

13. An interface for producing a monotonic signal for use by dynamic logic from a static logic signal, comprising:

a delay element; and,

a latch with an enable input, a clock input, a data input, and an output that produces said monotonic signal wherein said clock input is connected to a delay element input and said enable input is connected to a delay element output.

14. The interface of claim 13 wherein said latch is open until said clock input falls and said latch remains closed until a delay element delay after said clock input rises.

15. The interface of claim 14 wherein said clock input is coupled to an inverse of a dynamic logic evaluate clock.

16. The interface of claim 15 wherein said delay element is comprised of at least one inverter.